New Millennium Program Office
Microelectronics Systems

Microelectronics

Leon Alkalai, JPL

Dennis Andrucyk, GSFC

Presentation given by Jim Wall

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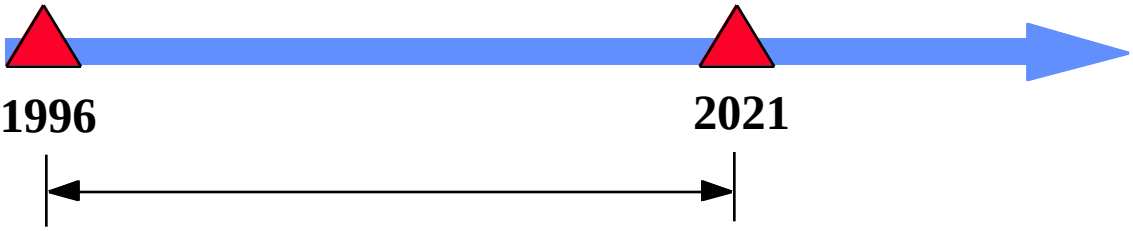
‘96 San Antonio Workshop

Microelectronics IPDT Report

James W. Wall
Jet Propulsion Laboratory
tel. 818 354-4588
email:james.wall@jpl.nasa.gov

Vision: The Next 25 years

Pentium Pro
P6



1996 **2021**

5.5 M Tr.

- System on a Chip
- Low-Power Electronics
- 3D VLSI Electronics
- Continued Performance Growth

Key Capability Needs for the 21st Century

- Develop reduction of all spacecraft electronics mass, volume and power by two orders of magnitude relative to the state-of-the art in space flight computing
- Accelerated insertion of commercial technology, components, and processes into space flight applications for the reduction of the total spacecraft life-cycle cost
- Scaleable and fault-tolerant on-board computing architectures that will enable autonomous spacecraft control and operation, and on-board science data analysis, for the the purpose of reducing the total system cost, and increase the mission scientific return.

Candidate High-Priority Technologies

- Highly integrated and modular 3D avionics architectures amenable to industry standardization
- Integrated power management electronics
- Advanced microelectronics packaging technologies such as Multichip Modules (MCMs), 3d chip stacking, and MCM stacking
- Low power electronics
- High-density low-power data storage technology
- High-bandwidth low-power interfaces
- Scaleable on-board real-time and reliable multiprocessing
- Fault tolerant computing
- Techniques for rapid prototyping

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IPDT NMP Flight Support Status

NMP Validation Flight	Candidate Technology Selection	Microelectronics System Architecture	IPDT Tasks Remaining
DS1	Complete	Near-Complete	Delivery of MCMs, Test & Integration, Delivery of Microelectronics Stack
DS2	Near-Complete	Near-Complete	General Support & Review
DS3	Preliminary	Preliminary	All Phases (Selection, Architecting, Delivery)
EO1	Late-Preliminary	Preliminary	Finalize Selection, Architecting, Delivery
EO2	Preliminary	Preliminary	All Phases
EO3	Preliminary	Preliminary	All Phases

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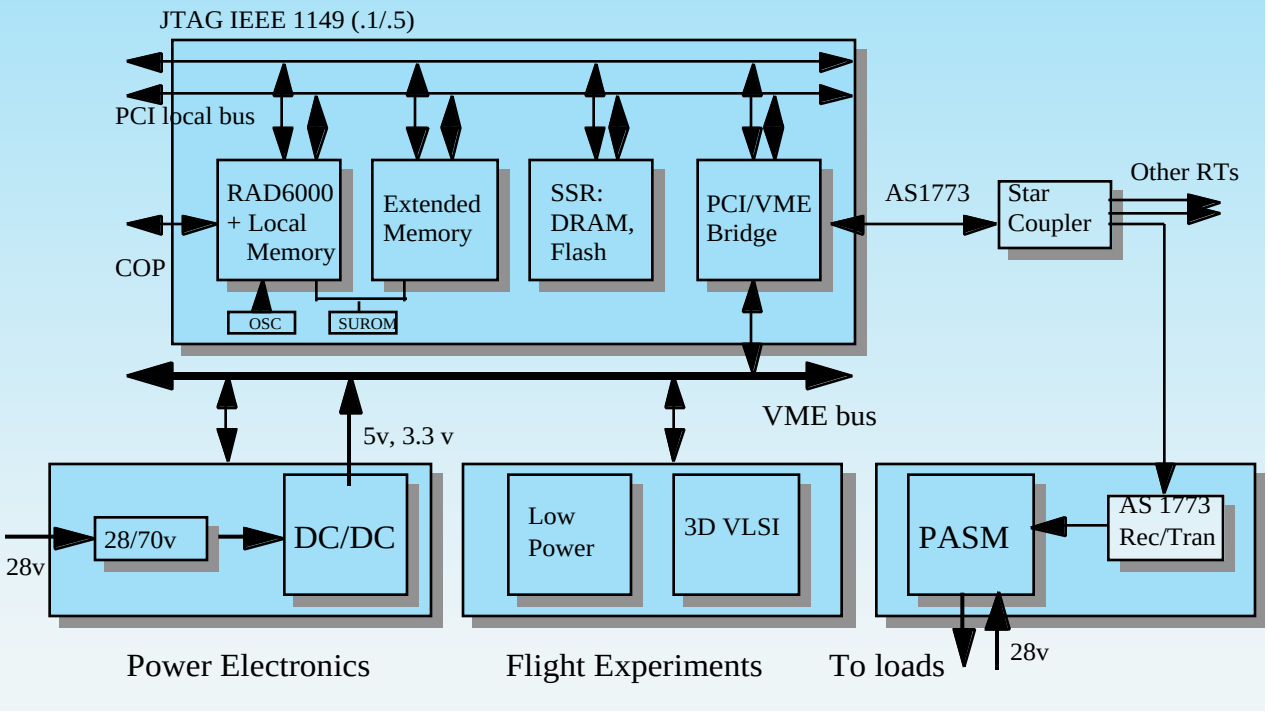
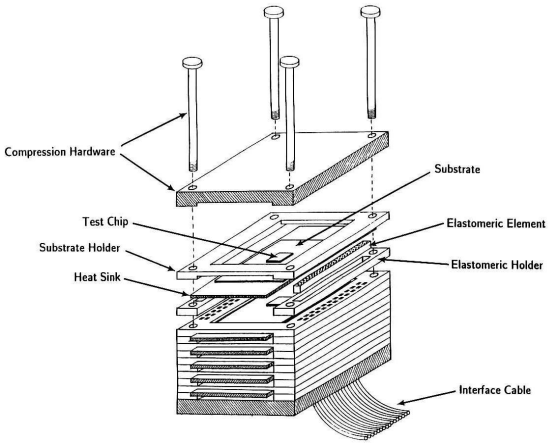
Proposed μE IPDT Technologies For DS1

DS1 Target Architecture



3D MCM Stacking

- Space Computer Corporation 3D MCM stacking technology
- Technology developed by BMDO
- Prototyped, validated in lab. and delivered sponsor.
- Program canceled due to $ cuts
- Mechanical tests and Electrical tests are encouraging
- TRL = 6; however, concerns remain for testability and reworkability.
- Partnership: SCC, BMDO, NASA
- Users: General purpose 3D avionics
- Benefits: eliminates backplane architecture, 10-100x reduction in mass and voluem relative to PCB.



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Proposed µE IPDT Technologies for DS2

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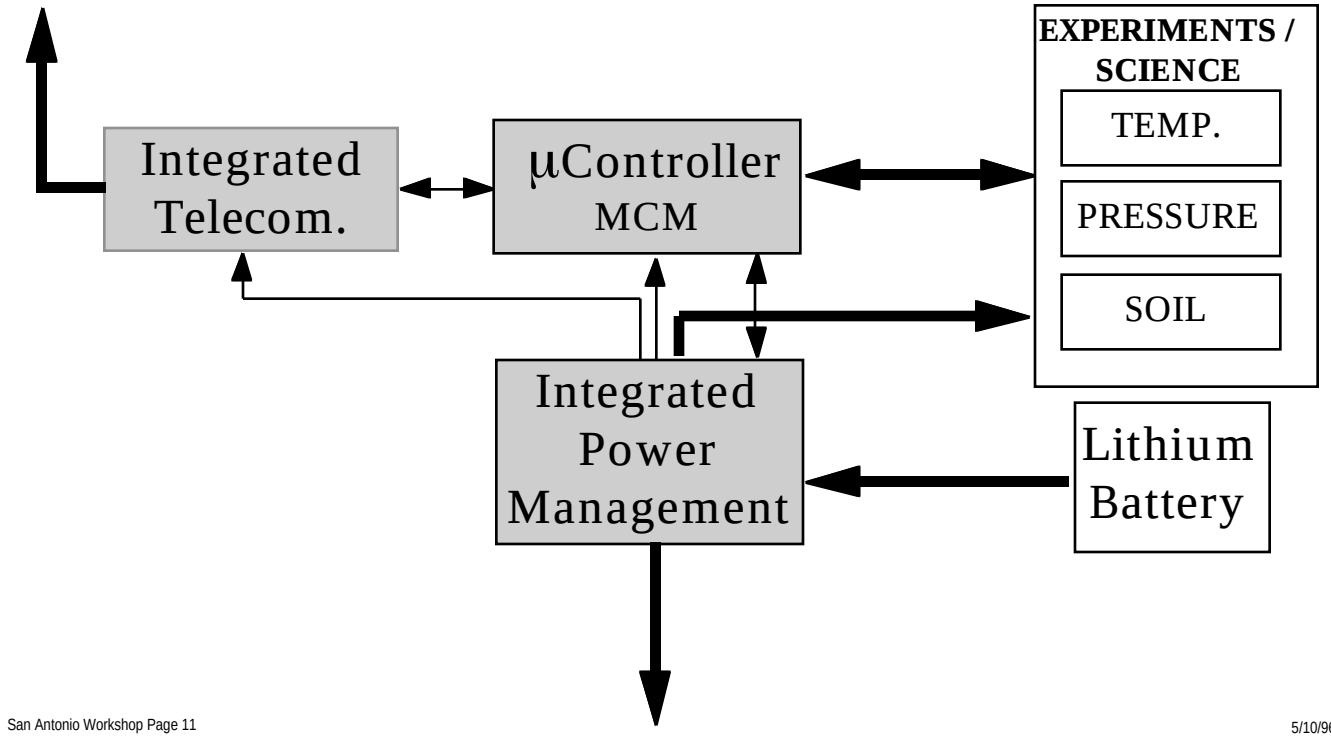
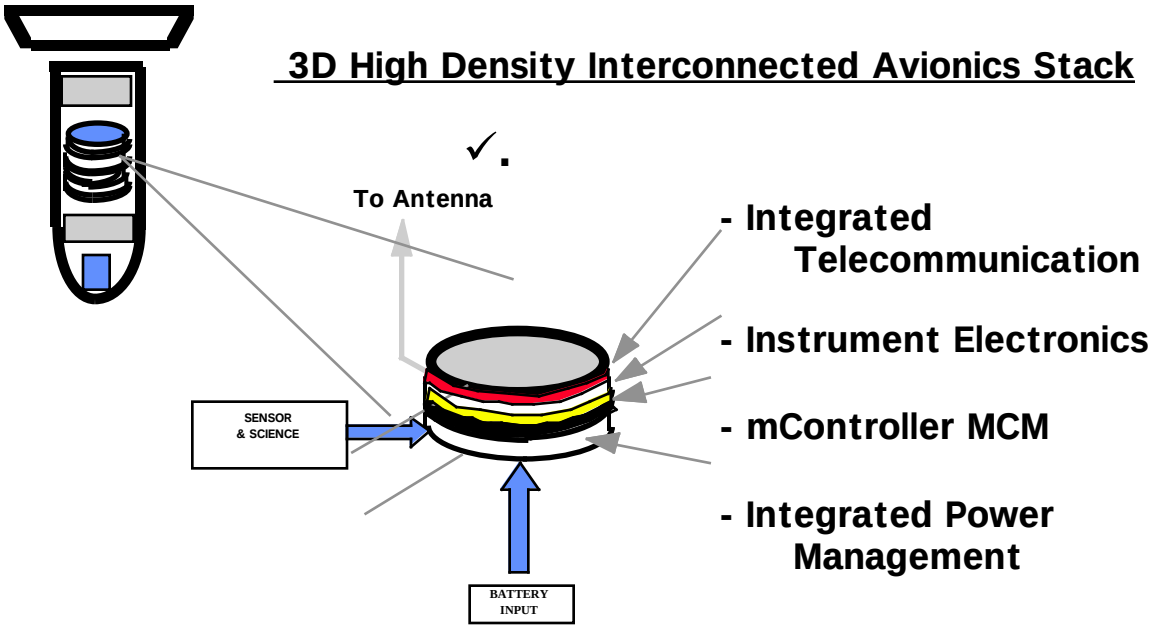
N M P

DS2 Target Architecture



3D High Density Interconnected Avionics Stack



- Integrated Telecommunication
- Instrument Electronics
- mController MCM
- Integrated Power Management

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Proposed μE IPDT Technologies For EO1

Command & Data Handling Technology	Mass (Kg)	Power (W)	Perfor-mance
Rad-Hard PowerPC CPU + Memory	0.2	5	55 MIPS
192 Gbit Solid State Recorder	1.5	4.5	192 Gbit
Fiber Optics Data Bus (FODB)	≈0.1	3.3	300 Mbps
3-D Packaging		N/A	N/A
DC-DC Converter	≈0.1		**80-90% efficient**
Power Activation & Switching Module	≈0.1		16 switch
Ultra Low Power Experiment	≈0.1		

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Summary of µElectronics Systems TRR

Technology Item	TRL
RAD6000-5L, CPU MCM	6
RAD6000-5L, Mem. MCM	6
RAD6000-5L, 3D cube	5
SSR, 3D Flash/DRAM	5
I/O AS 1773 I/F	7
Power HDI	5
Mixed Signal ASICs PASM	5
3D MCM Stacking	6

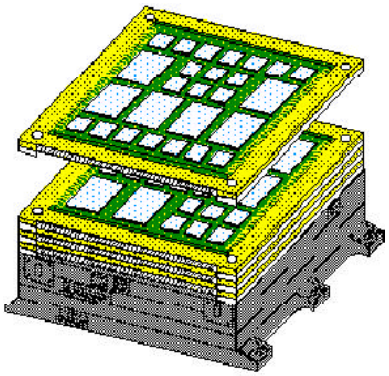
Pluto Express

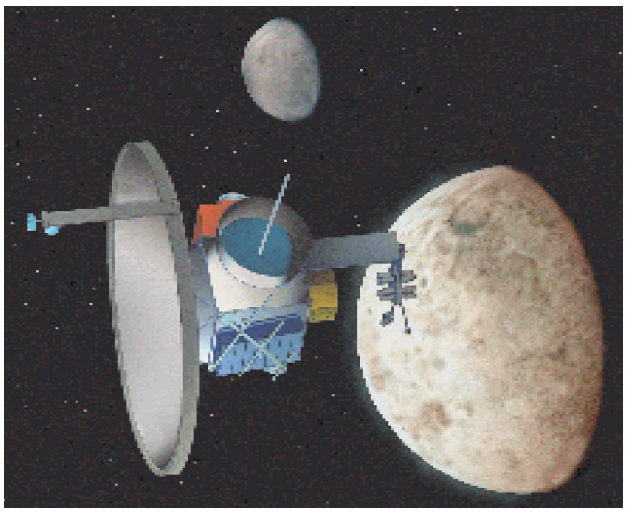
Reliability

Low Power

Fault Tolerance

Miniaturization





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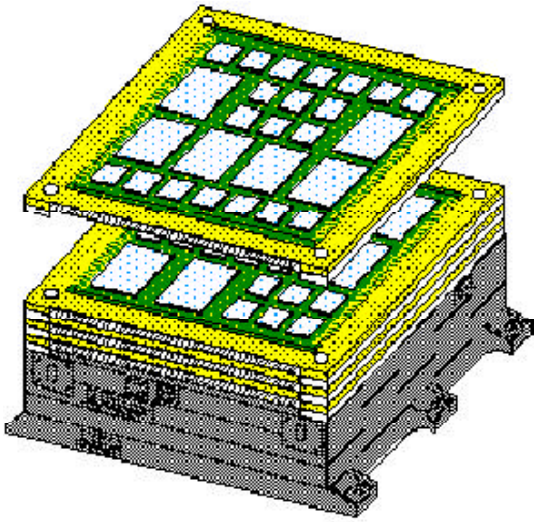
Advanced Avionics Technology for Reusable Launch Vehicles



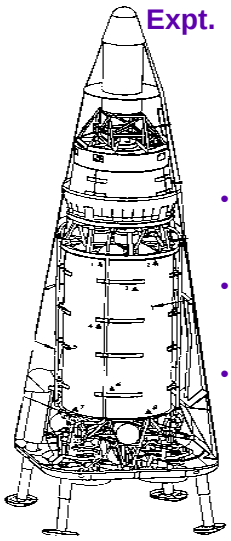
Reliability

Test and Maintenance

Fault Tolerance

Miniaturization

RI & MD
DC-XA LH2 Tank Expt.



- **Passive AU & AE sensors (60-500 KHz)**
- **Acoustic environment 150-170dB**
- **Severe cryoshock & vibration exposure**